What is claim d is:

1. A semiconductor integrated circuit comprising:

a unit cell array including a plurality of logic unit cells for providing general circuits and a plurality of clock unit cells for providing clock drivers;

a power trunk line formed on a peripheral area of the unit cell array, the power trunk line supplying a power source potential;

a plurality of first power branch lines formed on the unit cell array for supplying the power source potential to the logic unit cells, the first power branch lines connected each other and connected to the power trunk line; and

a plurality of second power branch lines formed on the unit cell array for supplying the power source potential to the clock unit cells, the second power branch lines connected each other and connected to the power trunk line.

2. A semiconductor integrated circuit according to claim 1, wherein the first power blanch lines includes a first column power blanch line and a first low power blanch line connected to the first column power blanch line at an intersection thereof.

3. A semiconductor integrated circuit according to claim 1, wherein the second power blanch lines includes a second column power blanch line and a second low power blanch line connected to the second column power blanch

line at an intersection thereof.

4. A semiconductor integrated circuit according to claim 1, wherein each of the logic unit cells has a plurality of transistors.

5. A semiconductor integrated circuit according to claim 4, wherein the transistors include a plurality of PMOS transistors and a plurality of NMOS transistors.

6. A semiconductor integrated circuit according to claim 1, wherein each of the clock unit cells has a plurality of transistors.

7. A semiconductor integrated circuit according to claim 6, wherein the transistors include a plurality of PMOS transistors and a plurality of NMOS transistors.

8. A semiconductor integrated circuit according to claim 1, further comprising an I/O circuit formed on an outer peripheral area of the power trunk line.

9. A semiconductor integrated circuit comprising:

a unit cell array including a plurality of logic unit cells for providing general circuits and a plurality of clock unit cells for providing clock drivers;

a first power trunk line formed on a peripheral area of the unit cell array, the first power trunk line supplying a power source potential;

a second power trunk line formed on the peripheral area, the second power trunk line supplying the power source potential, the first and second power trunk line being disconnected in the peripheral area;

a plurality of first power branch lines formed on the unit cell array for supplying the power source potential to the logic unit cells, the first power branch lines connected each other and connected to the first power trunk line; and

a plurality of second power branch lines formed on the unit cell array for supplying the power source potential to the clock unit cells, the second power branch lines connected each other and connected to the second power trunk line.

10. A semiconductor integrated circuit according to claim 9, wherein the first power blanch lines includes a first column power blanch line and a first low power blanch line connected to the first column power blanch line at an intersection thereof.

11. A semiconductor integrated circuit according to claim 9, wherein the second power blanch lines includes a second column power blanch line and a second low power blanch line connected to the second column power blanch line at an intersection thereof.

12. A semiconductor integrated circuit according to claim 9, wherein each of the logic unit cells has a plurality of transistors.

13. A semiconductor integrated circuit according to claim 12, wherein the transistors include a plurality of PMOS transistors and a plurality of NMOS transistors.

14. A semiconductor integrated circuit according

to claim 9, wherein each of the clock unit cells has a plurality of transistors.

15. A semiconductor integrated circuit according to claim 14, wherein the transistors include a plurality of PMOS transistors and a plurality of NMOS transistors.

16. A semiconductor integrated circuit according to claim 9, further comprising an I/O circuit formed on an outer peripheral area of the power trunk line.

17. A semiconductor integrated circuit comprising:

a unit cell block having a plurality of unit cells disposed in matrix form, the unit cell block having a plurality of logic unit cells for providing general circuit and a plurality of clock unit cells for providing clock drivers;

a first power branch line provided along a row direction of the matrix, the first power branch line supplying a source potential and a ground potential to the logic unit cells;

a second power branch line provided along the row direction, the second power branch line supplying the source potential and the ground potential to the clock unit cells; and

a power trunk line connected to ends of the first power branch line and the second power branch line.

18. A semiconductor integrated circuit according to claim 17, further including,

a third power branch line for supplying the source

potential and the ground potential to the logic unit cells, the third power branch line being provided along a column direction of the matrix and having an end connected to the power trunk line, and

a fourth power branch line for supplying the source potential and the ground potential to the clock unit cells, said fourth power branch line being provided along the column direction and having an end connected to the power trunk line.

19. A semiconductor integrated circuit according to claim 17, wherein the power trunk line includes,

a first power trunk line connected to the end of either one of the first power branch line and the third power branch line, and

a second power trunk line connected to the end of either one of the second power branch line and the fourth power branch line.

20. A semiconductor integrated circuit according to claim 19, wherein the source potential supplied by the second power trunk line is lower than the source potential supplied by the first power trunk line.

21. A semiconductor integrated circuit according to claim 19, further including a level shift circuit for generating the clock signal supplied to the general circuits.